

Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

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Listing of the Claims

Claims 1-42 (canceled)

- 10 43. (currently amended) A chip structure comprising:
- a silicon substrate;
 - a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;
 - a MOS device comprising a portion in said silicon substrate;
 - 15 a metallization structure over said silicon substrate, wherein said metallization structure ~~comprise~~ comprises a first metal layer and a second metal layer over said first metal layer;
 - a first dielectric layer between said first and second metal layers;
 - a passivation layer over said metallization structure and over said first dielectric
 - 20 layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure, ~~and exposes~~ and is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, ~~and exposes~~ and is at a bottom of said second opening, wherein said first and second contact points are separated from
 - 25 each other by an insulating material, ~~and~~ and wherein said passivation layer comprises silicon-
an insulating nitride layer; and
 - a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through

said circuit trace, and wherein said circuit trace is connected to said resistor through said first opening.

44. (previously presented) The chip structure as claimed in claim 43, wherein said dopant
5 comprises boron.

45. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises phosphorous.

10 46. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises arsenic.

47. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises gallium.
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48. (currently amended) The chip structure as claimed in claim 43 further comprising a polymer layer on between said passivation layer, ~~and wherein~~ said circuit trace is further on said polymer layer.

20 49. (previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises polyimide (PI).

50. (previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises benzocyclobutene (BCB).
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51. (currently amended) The chip structure as claimed in claim 43 further comprising a polymer layer on said circuit trace and over said passivation layer.

52. (previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises polyimide (PI).

5 53. (previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises benzocyclobutene (BCB).

54. (previously presented) The chip structure as claimed in claim 43 further comprising an inductor over said passivation layer.

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55. (previously presented) The chip structure as claimed in claim 54, wherein said inductor comprises a copper layer.

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56. (previously presented) The chip structure as claimed in claim 54, wherein said inductor comprises a gold layer.

57. (currently amended) The chip structure as claimed in claim 54, wherein said inductor comprises ~~a copper layer and a titanium-containing layer~~ and under said a copper layer over said titanium-containing layer.

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58. (currently amended) The chip structure as claimed in claim 57, wherein said titanium-containing layer comprises a titanium-tungsten alloy. ~~tungsten.~~

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59. (currently amended) The chip structure as claimed in claim 43 further comprising a capacitor over said silicon substrate, wherein said capacitor comprises a first electrode over said silicon substrate, wherein a third opening in said passivation layer is over said first electrode, and said first electrode has a top surface at a bottom of said third opening, a second electrode over said top surface, ~~said first electrode,~~ and a second dielectric layer

between said top surface ~~said first~~ and said second electrode, ~~electrodes, wherein a third opening in said passivation layer is over said first electrode and exposes said first electrode.~~

5 60. (previously presented) The chip structure as claimed in claim 59, wherein said second electrode comprises a gold layer.

61. (previously presented) The chip structure as claimed in claim 60, wherein said second electrode further comprises a titanium-containing layer under said gold layer.

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62. (previously presented) The chip structure as claimed in claim 59, wherein said second electrode comprises a copper layer.

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63. (previously presented) The chip structure as claimed in claim 59, wherein said second electrode comprises a copper layer and a nickel layer over said copper layer.

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64. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a

dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

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a passivation layer over said metallization structure and over said dielectric layer,

wherein a first opening in said passivation layer is over a first contact point of said

metallization structure, and ~~exposes said first contact point~~ is at a bottom of said first

opening, and wherein a second opening in said passivation layer is over a second contact

point of said metallization structure, and ~~exposes~~ said second contact point is at a bottom of said second opening, wherein said first and second contact points are separated from each other by an insulating material, ~~and~~ wherein said passivation layer comprises ~~silicon~~ an insulating nitride layer; and

5 a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

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65. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises boron.

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66. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises phosphorous.

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67. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises arsenic.

68. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises gallium.

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69. (currently amended) The chip structure as claimed in claim 64 further comprising a polymer layer ~~between~~ on said passivation layer, ~~and wherein~~ said circuit trace is further on said polymer layer.

70. (previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises polyimide (PI).

71. (previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises benzocyclobutene (BCB).

5 72. (currently amended) The chip structure as claimed in claim 64 further comprising a polymer layer on said circuit trace and over said passivation layer.

73. (previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises polyimide (PI).

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74. (previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises benzocyclobutene (BCB).

Claims 75-82 (canceled)

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83. (currently amended) The chip structure as claimed in claim 64, wherein said titanium-containing layer comprises a titanium-tungsten alloy. ~~tungsten.~~

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84. (previously presented) The chip structure as claimed in claim 64, wherein said metallization structure comprises aluminum.

Claims 85-88 (canceled)

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89. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer,

5 wherein a first opening in said passivation layer is over a first contact point of said metallization structure, ~~and exposes said first contact point~~ is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said metallization structure, ~~and exposes said second contact point~~ is at a bottom of said second opening, wherein said first and second contact points are separated from
10 each other by an insulating material, ~~and wherein said passivation layer comprises silicon~~ an insulating nitride layer; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first
15 opening, and wherein said circuit trace comprises a copper layer.

90. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises boron.

20 91. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises phosphorous.

92. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises arsenic.

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93. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises gallium.

94. (currently amended) The chip structure as claimed in claim 89 further comprising a polymer layer ~~between-on~~ said passivation layer, ~~and wherein~~ said circuit trace is further on said polymer layer.

5 95. (previously presented) The chip structure as claimed in claim 94, wherein said polymer layer comprises polyimide (PI).

96. (previously presented) The chip structure as claimed in claim 94, wherein said polymer layer comprises benzocyclobutene (BCB).

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97. (currently amended) The chip structure as claimed in claim 89 further comprising a polymer layer on said circuit trace and over said passivation layer.

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98. (previously presented) The chip structure as claimed in claim 97, wherein said polymer layer comprises polyimide (PI).

99. (previously presented) The chip structure as claimed in claim 97, wherein said polymer layer comprises benzocyclobutene (BCB).

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100. (previously presented) The chip structure as claimed in claim 89, wherein said circuit trace further comprises a nickel layer over said copper layer.

101. (previously presented) The chip structure as claimed in claim 89, wherein said circuit trace further comprises a gold layer over said copper layer.

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102. (previously presented) The chip structure as claimed in claim 89, wherein said circuit trace further comprises a nickel layer over said copper layer, and a gold layer over said nickel layer.